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EXAMINER	
NGUYEN, TRONG H	
ART UNIT	**PAPER NUMBER**
2436	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/559,917	ROTTSCHAFER ET AL.	
	Examiner	Art Unit	
	TRONG NGUYEN	2436	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) *1,3,9,11,12 and 14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the communication filed on 12/10/2008. In response to the office action mailed on 10/17/2008, claims **1-17** have been amended. Pending claims include claims **1-17**.

Response to Arguments

2. Applicant's arguments with respect to claims **1 and 11** have been considered but are moot in view of new ground(s) of rejection.

Furthermore, examiner would like to clarify the mappings regarding the claimed control device and round key generation means. As seen on pages 6-7 of previous office action, selection **24**, selector **25** and step counter **26** are mapped to the claimed control device while address calculating circuit **23** and magnification key latch **7** are mapped to the claimed key generation means. Hence, address calculating circuit **23** is not mapped to both the claimed control device and the claimed key generation means as argued by applicant.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because the abstract in the instant application exceeds the maximum 150 word limit and includes the legal phraseology of "means". Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claim **1** is objected to because of the following informalities: Claim **1** recites "the storage device" in line 11. There is insufficient antecedent basis for this limitation in the claim. Moreover, claim **1** recites "the data" in line 14. There is insufficient antecedent basis for this limitation in the claim.

Claim **3** is objected to because of the following informalities: Claim **3** recites "the same physical path" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim **9** is objected to because of the following informalities: Claim **9** recites "the data" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim **11** recites "a round key generation means" in line 4, "at least one round key generation means" in lines 7-8. It appears that they both refer to the same thing. Hence, it is inconsistent. Reconsideration of claim language is suggested. For examining purposes, hereinafter, "a round key generation means" and "at least one round key generation means" will be considered to be referred to the same thing.

Claim **12** is objected to because of the following informalities: Claim **12** recites "between the control device with the at least one encryption/decryption means" in lines 2-3 which should be "between the control device and the at least one encryption/decryption means".

Claim **14** is objected to because of the following informalities: Claim **14** recites "the memory" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim **15** recites "the round key generation means" in line 2. It appears that "the round key generation means" refers to "the at least one round key generation means" in claim **11** and thus is inconsistent.

Claim **16** recites "the round key generation means" in lines 2-3. It appears that "the round key generation means" refers to "the at least one round key generation means" in claim **11** and thus is inconsistent.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims **1 and 4** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim **1** recites "the key generation means" in lines 5-6. There is insufficient antecedent basis for this limitation in the claim. Furthermore, it is unclear if "the key

generation means" refers to "round key generation means" or some other key generation means. For examining purposes, hereinafter, "the key generation means" will be considered as "round key generation means" recited in line 7 of claim **1**.

Claim **4** recites "wherein the at least one round key is temporarily stored" in line 3. It is unclear whether the at least one round key is temporarily stored in the memory of the control device or it is temporarily stored somewhere else. For examining purposes, hereinafter, "wherein the at least one round key is temporarily stored" will be considered as temporarily stored in the memory of the control device.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims **1**, **4**, **8**, **9**, **11**, **15**, and **16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui US 5,261,003 (hereinafter "Matsui") in view of Muratani et al. US 2002/0021802 (hereinafter "Muratani").

Regarding claim **1**, Matsui discloses "**A processor for encrypting and decrypting data comprising:**" as ["a data communication system with a data scrambling" (Col. 5, lines 44-45, Fig. 1)] "**a control device**" [selector 24, selector 25, and step counter 26 (Fig. 1)] "**is connected to at least one encryption/decryption**

means" [scramble processing means 33 (Fig. 1, Col. 5, line 65)] "**via at least one communication means**," [Fig. 1] "**wherein, the control device comprises a memory**" as [the extended key latch 7 supplies the selected extended key corresponding to the given address to the selector 25, and the key is transmitted to the processing block 9 through the selector 25 (Col. 6, lines 12-15)] "**and at least one external key input**" as [the magnification key latch 7 supplies the selected extended key to the selector 25 (Col. 6, lines 12-14, Fig. 1)] "**at least one round key generation means connected to the control device**" as [address calculating circuit 23 and magnification key latch 7 (Fig. 1)] "**via at least one further communication means**," as [Fig. 1] "**wherein the round key generation means receives a data word from the control device for calculating at least one round key**" as [First, the input plaintext 3 is divided into more significant 4 bytes and less significant 4 bytes, and the less significant 4 bytes are input to the processing block 9 and the address calculating circuit 23 through the selector 24. The address calculating circuit 23 calculates an address of a extended key to be selected on the basis of the input plaintext data and outputs the calculated address to the extended key latch 7 (Col. 6, lines 4-12). *Note that an extended key is generated by calculating its address based on the input plaintext data using the address calculating circuit 23. Thus, the calculated key is a function of the input plaintext. As disclosed by Matsui, since the content of the cipher key or the scramble function to be input to the processing block of each step can be varied depending on the content of the plaintext, high random rate can be obtained and thus the possibility of decoding or analysis of the data communication can be reduced (Col. 9, lines 63-68)*] "**and transfers the at least**

one round key to the memory of the storage device;" as [the extended key latch 7 supplies the selected extended key corresponding to the given address to selector 25 (Col. 6, lines 12-14, Fig. 1)] "**wherein the at least one encryption/decryption means comprises at least one external data input for receiving the data**," as [plaintext 3 (Fig. 1), selector 25 outputs selected extended keys to all of the scramble processing blocks 9-11 in scramble processing means 33 (Col. 6, lines 14-15, 34-36, Fig. 1)] "**an input for receiving the at least one round key from the memory of the control device**," as [selector 25 outputs selected extended keys to all of the scramble processing blocks 9-11 in scramble processing means 33 (Col. 6, lines 14-15, 34-36, Fig. 1)] "**and at least one external data output for outputting data processed with the at least one round key**," as [scrambled text 4 (Fig. 1)] "and **wherein the at least one encryption/decryption means and the at least one round key generation means communicate solely via the control device**" as [scramble processing means 33 and address calculating circuit 23 and magnification key latch 7 communicate solely using selector 24, selector 25 (Fig. 1)].

Matsui does not expressly disclose "**that receives an initial key from a source other than the key generation means**".

However, Muratani discloses an encryption apparatus, decryption apparatus and expanded key generation apparatus and method (Col. 2, Par. 0025, lines 1-3) wherein an initial key (expanded common key kc') is received by a control device (decoder 7 and switching circuit 15) other than a key generation means (expanded key scheduling section 3) (Fig. 16 and Col. 9, Pars. 0203 and 0204).

Muratani and Matsui are analogous art because they are in the same field of endeavor of data encryption/decryption.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Matsui's data communication system with a data scrambling by having the control device receives an initial key from a source other than the key generation means as described by Muratani since it would provide for the purpose of being effective in view of safety against attack (Muratani, Col. 9, Par. 0207).

Regarding claim **4**, Matsui in view of Muratani discloses "**The processor of claim 1, wherein the at least one round key is temporarily stored**" as [the extended key latch 7 supplies the selected extended key to the selector 25 and the key is then transmitted to the processing block 9 (Matsui, Col. 6, lines 12-15)].

Regarding claim **8**, Matsui in view of Muratani discloses "**The processor of claim 1, wherein the round key generation means is adapted to perform a dummy operation**" as [Although exemplary configurations of FIG. 1 and FIG. 2 generate a plurality of expanded keys in number required for the data randomizing section, there can comprise the number of stages for round functions capable of generating expanded keys in number that exceeds the number required for the data randomizing section, wherein a part of the generated expanded keys is used by the data randomizing section (Muratani, Col. 8, Par. 0178). Note that non-used expanded keys are dummy operations as Muratani discloses that a configuration in which only part of the expanded keys that are capable of being generated is used for data randomizing is effective in view of safety against attack (Muratani, Col. 8, Par. 0185)].

Regarding claim **9**, Matsui in view of Muratani discloses "**The processor of claim 1, wherein a time between the calculating of the at least one round key by the round key generation means and the processing of the data using the at least one round key is variable**" as [Muratani discloses that the order in which the expanded keys are generated may be changed, for example, an earlier generated expanded key may be temporarily stored in a memory to be used later than a later generated expanded key (Fig. 15, Col. 9, Par. 0197, lines 4-5, Par. 0199, lines 1-3)].

Regarding claim **11**, Matsui discloses "**A method of encrypting and/or decrypting data using a processor comprising**:" as [a data communication method with a data scrambling (Col. 4, lines 5-6)] "**a) at least one initial key is read into a control device**" as [the magnification key latch 7 supplies the selected extended key to the selector 25 (Col. 6, lines 12-14, Fig. 1)] "**b) external data are read into at least one encryption/decryption means**" as [plaintext 3 (Fig. 1), selector 25 outputs selected extended keys to all of the scramble processing blocks 9-11 in scramble processing means 33 (Col. 6, lines 14-15, 34-36 Fig. 1)] "**c) at least one data word needed to calculate at least one round key is read from at least one storage means of the control device and transferred to at least one round key generation means**" as [the less significant 4 bytes of plaintext data are input to the address calculating circuit 23 through the selector 24 (Col. 6, lines 6-8)] "**at least one round key is calculated on the basis of the at least one data word by means of the at least one round key generation means, transferred to the control device and stored in the at least one storage means**" as [the address calculating circuit 23 calculates an address of an

extended key to be selected on the basis of the input plaintext data and outputs the calculated address to the extended key latch 7 (Col. 6, lines 8-12, Fig. 1) and the extended key latch 7 supplies the selected extended key corresponding to the given address to selector 25 (Col. 6, lines 12-14, Fig. 1). *Note that an extended key is generated by calculating its address based on the input plaintext data using the address calculating circuit 23. Thus, the calculated key is a function of the input plaintext. As disclosed by Matsui, since the content of the cipher key or the scramble function to be input to the processing block of each step can be varied depending on the content of the plaintext, high random rate can be obtained and thus the possibility of decoding or analysis of the data communication can be reduced (Col. 9, lines 63-68)*] "**e) the at least one round key is transferred from the at least one storage means to the at least one encryption/decryption means**" as [selector 25 outputs selected extended keys to scramble processing blocks 9-11 in scramble processing means 33 (Col. 6, lines 14-15, 34-36, Fig. 1)] "**f) the external data are processed by means of the at least one encryption/decryption means using the at least one round key**" as [scramble processing means 3 scrambles an input data by using an extended key to output a scrambled data (Col. 6, lines 15-17, 36-39, Fig. 1)] "**and the processed data are made available at at least one external data output**," as [scrambled text 4 (Col. 6, lines 44-48, Fig. 1)] "**g) steps b) to f) are repeated as often as necessary to encrypt or decrypt a set of external data**" as [the same processing as described above is repeated predetermined times to produce scrambled text 4 (Col. 6, lines 44-48)].

Matsui does not expressly disclose "**wherein the at least one initial key is obtained from a source other than a round key generation means**" and "**round key is calculated recursively**".

However, Muratani discloses an encryption apparatus, decryption apparatus and expanded key generation apparatus and method (Col. 2, Par. 0025, lines 1-3) wherein an initial key (expanded common key kc') is received by a control device (decoder 7 and switching circuit 15) other than a key generation means (expanded key scheduling section 3) (Fig. 16 and Col. 9, Pars. 0203 and 0204). Moreover, Muratani discloses a key generation method wherein round keys are generated recursively on the basis of previous sub keys (Fig. 1).

Muratani and Matsui are analogous art because they are in the same field of endeavor of data encryption/decryption.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Matsui's data communication system with a data scrambling by having the control device receives an initial key from a source other than the key generation means and calculating round key recursively as described by Muratani since it would provide for the purpose of being effective in view of safety against attack (Muratani, Col. 8, Par. 0185, line 3 and Col. 9, Par. 0207).

Regarding claim **15**, this claim contains limitations that are substantially similar to those recited in claim **8** above and accordingly is rejected for the same reasons.

Regarding claim **16**, this claim contains limitations that are substantially similar to those recited in claim **9** above and accordingly is rejected for the same reasons.

9. Claims **2-3**, **6-7**, and **12-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui in view of Muratani and further in view of John L. Hennessy and David A. Patterson, Computer Architecture: A Quantitative Approach, 2nd ed., Morgan Kaufmann, January 1996 (hereinafter "Hennessy and Patterson").

Regarding claim **2**, Matsui in view of Muratani discloses "**The processor of claim 1**," but does not expressly disclose "**wherein the at least one communication means comprises at least one request line, at least one release line and at least one data line and the at least one further communication means comprises at least one further request line, at least one further release line and at least one further data line**".

However, Hennessy and Patterson disclose an asynchronous bus comprising a request line, an acknowledgement line, and a data line (Page 499, Fig. 6.11).

Hennessy and Patterson, Matsui, and Muratani are analogous art because they are in the same field of endeavor of computer architecture and data communication.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the data communication system with a data scrambling of Matsui in view of Muratani by including an asynchronous bus as described by Hennessy and Patterson since it would be much easier to accommodate a variety of devices and to lengthen the bus without worrying about clock skew or synchronization problems (Hennessy and Patterson, Page 499, Par. 3, lines 1-3).

Regarding claim **3**, Matsui in view of Muratani discloses "**The processor of claim 1**," but does not expressly disclose "**characterized in that the at least one request line, the at least one release line and the at least one data line and the at least one further request line, the at least one further release line and the at least one further data line at least partially use the same physical path**".

However, Hennessy and Patterson disclose an asynchronous bus comprising a request line, an acknowledgement line, and a data line (Page 499, Fig. 6.11).

Hennessy and Patterson, Matsui, and Muratani are analogous art because they are in the same field of endeavor of computer architecture and data communication.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the data communication system with a data scrambling of Matsui in view of Muratani by including an asynchronous bus as described by Hennessy and Patterson since it would be much easier to accommodate a variety of devices and to lengthen the bus without worrying about clock skew or synchronization problems (Hennessy and Patterson, Page 499, Par. 3, lines 1-3).

Regarding claim **6**, Matsui in view of Muratani discloses "**The processor of claim 1**," but does not expressly disclose "**wherein the communication between the control device and the at least one encryption/decryption means and between the control device and the at least one round key generation means is accomplished using at least one handshake protocol**".

However, Hennessy and Patterson disclose an asynchronous bus wherein "self-timed, handshaking protocols are used between bus sender and receiver" (Page 499, Par. 2, lines 1-2).

Hennessy and Patterson, Matsui, and Muratani are analogous art because they are in the same field of endeavor of computer architecture and data communication.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the data communication system with a data scrambling of Matsui in view of Muratani by using handshaking protocols as described by Hennessy and Patterson since it would be much easier to accommodate a variety of devices and to lengthen the bus without worrying about clock skew or synchronization problems (Hennessy and Patterson, Page 499, Par. 3, lines 1-3).

Regarding claim **7**, Matsui in view of Muratani discloses "**The processor of claim 1**," but does not expressly disclose "**wherein the operation of the of the control device, of the at least one encryption/decryption means and of the at least one round key generation means are asynchronous with respect to one another**".

However, Hennessy and Patterson disclose an asynchronous bus wherein "self-timed, handshaking protocols are used between bus sender and receiver" (Page 499, Par. 2, lines 1-2).

Hennessy and Patterson, Matsui, and Muratani are analogous art because they are in the same field of endeavor of computer architecture and data communication.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the data communication system with a data scrambling of Matsui

in view of Muratani by including an asynchronous bus as described by Hennessy and Patterson since it would be much easier to accommodate a variety of devices and to lengthen the bus without worrying about clock skew or synchronization problems" (Hennessy and Patterson, Page 499, Par. 3, lines 1-3).

Regarding claim **12**, this claim contains limitations that are substantially similar to those recited in claim **6** above and accordingly is rejected for the same reasons.

Regarding claim **13**, this claim contains limitations that are substantially similar to those recited in claim **7** above and accordingly is rejected for the same reasons.

10. Claims **5** and **14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui in view of Muratani and further in view of Tran US 5,919,251 (hereinafter "Tran").

Regarding claim **5**, Matsui in view of Muratani discloses "**The processor of claim 1**," but does not expressly disclose "**wherein the at least one round key from the memory of the control device is accessed using a rotating pointer**".

However, Tran discloses a rotating pointer buffer for storing data in integrated circuits wherein a head pointer and a tail pointer are used to provide access (Col. 1, lines 51, 54-47, Fig. 1).

Tran, Matsui, and Muratani are analogous art because they are in the same field of endeavor of data storage.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify data communication system with a data scrambling of Matsui in view of Muratani by including at least one rotating pointer to provide access to storage

areas in selectors as described by Tran since rotating pointer structure is superior to shifting structure in terms of lowest area consumption and speed (Tran, Col. 2, lines 18-20, Table 1).

Regarding claim **14**, this claim contains limitations that are substantially similar to those recited in claim **5** above and accordingly is rejected for the same reasons.

11. Claims **10** and **17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui in view of Muratani and further in view Verbauwhede US 2003/0202658 (hereinafter "Verbauwhede").

Regarding claim **10**, Matsui in view of Muratani discloses "**The processor of claim 1**," but does not disclose "**wherein the processor is an AES coprocessor**".

However, Verbauwhede discloses AES architecture for encrypting or decrypting data (Col. 1, Par. 0007, line 1).

Verbauwhede, Matsui, and Muratani are analogous art because they are in the same field of endeavor of data encryption/decryption.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the data communication system with a data scrambling of Matsui in view of Muratani to be an AES architecture as described by Verbauwhede in order to achieve a high data rate (Verbauwhede, Col. 1, Par. 0006, lines 1-2).

Regarding claim **17**, this claim contains limitations that are substantially similar to those recited in claim **10** above, and accordingly is rejected for the same reasons.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG NGUYEN whose telephone number is (571)270-7312. The examiner can normally be reached on Monday through Thursday 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NASSER MOAZZAMI can be reached on (571)272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T.N./

/Nasser G Moazzami/
Supervisory Patent Examiner, Art Unit 2436